FACULTY PROFILE

1. Personal Details

NAME	**Mrs. RAJESHWARI BHAT**	
DEPARTMENT	ELECTRONICS & COMMUNICATION ENGINEERING	
DESIGNATION	ASSISTANT PROFESSOR	
PHONE	9650097526	
EMAIL ID	rajeshwaribhat2@jssaten.ac.in	
Date of Joining (JSSATEN)	01- 08-2013	

2. Experience

Total Experience in Years: 10	Teaching: 10	Industry: Nil	Research:

3. Qualifications

COURSES	SPECIALIZATION	Year of Award	INSTITUTION	UNIVERSITY
B.E.	Electronics and Communication Engineering.	1995	BVB college of Engg. And Tech. Hubli	Karnataka University, Dharwad
M. Tech.	VLSI Design	2012	JSS Academy of Technical Education, Noida	GBTU, Lucknow
Ph.D.	VLSI Design	Pursuing	Galgotias University, Greater Noida	Galgotias University, Greater Noida
Post Doc.	-	-	-	-

4. Research & Publications

Papers Published in Web of Science indexed Journals	International: 00	National: 00
Papers Published in SCOPUS indexed	International: 02	National: 00

Journals		
Papers Published in other Journals	International: 00	National: 00
Papers Presented in Conferences / Symposium	International: 01	National: 00
Books / Book chapters Published	Name of the book: NIL Publisher: Year of Publication:	

5. Research Guidance

PhD Guide? Give field & University	No	NA
Ph.D.s / Projects Guided	Ph.D. Awarded: No Guiding: NIL	Projects at Master's Level: Nil Projects at Bachelor's Level: 24

6. Grants
i. Funds Received (Projects)

Project Name	Grant Amount	Date of receiving the Grant	Duration	Grant issuing authority/ Body / Organization
-	-	-	-	-

ii. Patents

Sl. No.	Title Details	Details of award of patent / Filed
-	-	-

iii. Consultancy

Title of the work	Amount in Rs.	Date of receiving the Grant	Duration	Grant issuing authority/ Body / Organization
-	-	-	-	-

7. Awards Received

Awards "Best Paper Award"	Nil

8. Publications
i. International Journals

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus / Both	Impact Factor	Publisher
1	Integrated power and clock distribution circuits in a wired and wireless clock network	Rajeshwari Bhat, Ruqaiya Khanam	IJITEE	Vol 8, Issue 7s, May 2019	Scopus	-	-
2	Effect of Integrated power and clock distribution networks on Combinational circuits	Rajeshwari Bhat, Ruqaiya Khanam, Mohammad Rashid Ansari	IJRES	Vol 9, Issue no. 3, Nov 2020	Scopus	-	-

ii. National Journals

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus / Both	Impact Factor	Publisher
-	-	-	-	-	-	-	-

iii. Conferences

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Conference	Volume No. Issue No. Year	WOS / Scopus	Impact Factor	Publisher
1	IPCDN circuit in a wired and wireless clock network. held at ABES Engineering college, Ghaziabad, UP in	Rajeshwari Bhat, Ruqaiya Khanam	International Conference on system modeling simulation and Intelligent Computing(ICSMSIC 2019)	Vol 8, Issue 7s, May 2019	Scopus	-	-

	March 2019						

iv. Workshops /Conferences Attended

Sl. No.	Name of the workshop / Conference	Organizer	Date
1	One Week Workshop on VLSI Device, Circuit and System Design Tools (Online)	School of Electronics Engineering (SENSE), VIT-AP University, Amaravati (AP)	June, 2022
2	Advanced VLSI Design and Applications with hands-on CADENCE Tools with subtopic Analog Integrated Circuit Design(online)	Department of Electronics & Communication Engineering, ABES Engineering College, Ghaziabad.	August, 2020
3	Indo-Muscat one-week Virtual workshop on Research Writing Skills	Galgotias University, India.	May, 2020
4	Two week FDP on Entrepreneurship Development	ABES Engineering college, Ghaziabad, UP	Jan , 2019
5	One week FDP on "Industrial Automation using Robotics and 3 D Printer"	JSS Academy of Technical Education , Noida	May 2018
6	One week Short term course on VLSI Design using ICT	JSS Academy of Technical Education, Noida	October 2015

v. Workshops / Conference (Organized)

Sl. No.	Name of the workshop / Conference	Organized by	Date	Role
-	-	-	-	-

vi. Conference Attended (those sponsored by AICTE / ISTE/IETE/TEQIP or any other sponsoring body)

Sl. No.	Name of the workshop / Conference	Organizer	Date
1	Two week FDP on "Entrepreneurship" (TEQIP)	ABES Engineering college, Ghaziabad, UP	Jan , 2019

9. Details of NPTEL / COURSERA courses completed

Sl. No.	Name of the subject	Organized by	Date of completion / Award	Grade / Marks
1	C based VLSI Design	NPTEL	October 2022	53/100

10. Membership of Professional Bodies:

1. Membership at IAENG- (229435)

11. Any other information you will like to share about your professional experience

-